



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q77404

Keiji HAYASHIDA, et al.

Appln. No.: 10/664,884

Group Art Unit: 2817

Confirmation No.: 4264

Examiner: Unknown

Filed: September 19, 2003

For: PHASE-LOCKED LOOP CIRCUIT REDUCING STEADY STATE PHASE ERROR

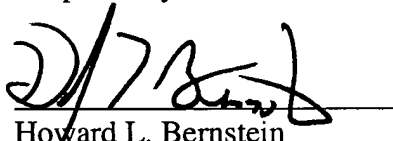
SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find 4 sheets of formal drawings in compliance with
37 C.F.R. § 1.84. The Examiner is respectfully requested to acknowledge receipt of these
drawings.

Respectfully submitted,


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Date: January 5, 2004